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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
OSBORNE, LUKE R	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/034,565	ANDRADE ET AL.	
	Examiner	Art Unit	
	Luke Osborne	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-108* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-108* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/1/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Status

1. Claims 1-108 are pending in the instant application.

Claims 1-108 stand rejected.

2. Applicant's arguments submitted 1/10/2006 have been fully considered, Examiners response is as follows.

Priority

3. Examiner acknowledges the argument regarding the support in the specification as filled for creating a block diagram. Consequently the objection is withdrawn.

Information Disclosure Statement

4. Examiner appreciates the submittal of the missing references since they were missing in the parent case file, as such they have been considered.

Claim Objections

5. Examiner acknowledges the amendment to claim 5. Consequently the objection is withdrawn.

6. Claims 1-108 are objected to because of the following reasons. Claim 1 as exemplary recites both "programmable hardware element" and "reconfigurable circuitry". It is uncertain to the Examiner what is separates the meets and bounds between the

"programmable hardware element" and "reconfigurable circuitry". Examiner requests Applicants' help in determining the difference as the specification does not provide an appropriate definition between these limitations.

Applicant's Argument

Applicant's point out page 3, line 13, of the specification provides specific distinctions and proper definitions between the limitations "programmable hardware element" and "reconfigurable circuitry".

Examiner's Response

Examiner finds this argument to be unpersuasive and the definitions provided at the specified locations insufficient to form a binding definition over which is generally known. As shown in page 3 of Applicant's specification and as argued on pages 32 and 33 of Applicant's response the definitions provided are purely exemplary. These definitions while helpful in ascertaining Applicant's specified invention provide no binding definition for the claimed limitations. Since there is no proper definition provided the ordinary meaning is used, as such there is significant overlap if not identical meanings between the limitations "programmable hardware element" and "reconfigurable circuitry", as the words programmable, and reconfigurable as found in IEEE 100 (Programmable: that characteristic of a device that makes it capable of accepting data to alter the state of its internal circuitry to perform a specific task(s)). With this definition of programmable "reconfigurable circuitry" is well within this definition from it's ordinary meaning.

Applicant's arguments would be persuasive if the programmable hardware element was an FPGA, and if the reconfigurable circuitry were front end reconfigurable transceivers, and such transceivers were configured using the hardware architecture file.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Examiner acknowledges the amendment to claim 23. Consequently the rejection is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claims 1-108 are rejected under 35 U.S.C. 103(a) as being unpatentable over A software development system for PFGA-based data acquisition systems by Wenban et al, hereinafter "Wenban" in view of Software advances in measurement and instrumentation, by Fountain hereinafter "Fountain".

Regarding claim 1, Wenban teaches a computer-implemented method for configuring a device to perform a measurement function, wherein the device includes a programmable hardware element, wherein the device also includes reconfigurable circuitry coupled to the programmable hardware element, see the abstract, and page 36 9- Conclusion for this teaching. Wenban further teaches, the method comprising:

generating a hardware architecture file based on at least a portion of the computer program, wherein the hardware architecture file describes a hardware implementation of the at least a portion of the computer program [Wenban: our compiler translates Promela into register transfer level AHDL or EDIF code (Page 28, right column)];

configuring the programmable hardware element in the device utilizing the hardware architecture file, wherein after said configuring the programmable hardware element implement a hardware implementation of the at least a portion of the computer program [Wenban: page 33, 6 Interfaces];

configuring the reconfigurable circuitry in the device [Wenban: A complete FPGA configuration file can be downloaded over the network in to the SRAM using these messages (Page 36, left column, second paragraph)];

the device acquiring a signal from an external source after said configuring [Page 35, last paragraph before 9 conclusion]; and the programmable hardware element and the reconfigurable circuitry in the device executing to perform the measurement function on the signal.

Wenban does not expressly teach that the computer program is written as a block diagram.

Fountain teaches national instruments Lab View, which teaches the use of block diagrams for a familiar technique and to enable rapid building, testing and modifying on page 8.

It would have been obvious to one of ordinary skill in the art at the time of applicants invention to combine the graphical programming of Fountain with the development environment of Wenban.

The motivation for doing so would have been as discussed above to create a familiar technique and to enable rapid building, testing and modifying on Fountain on page 8.

Applicant's Argument

Applicant respectfully submits that Weban nowhere teaches reconfigurable circuitry coupled to the programmable hardware element.

Examiners Response

Without a clear definition of the claim limitations are given their broadest reasonable interpretation under MPEP §2111. Applicant's arguments are not in commensurate scope with the claimed invention. As explained above in the objection to the limitations that Applicant's seek to distinguish. Furthermore on page 34 of Applicant's response Applicant's discuss the Weban reference and highlight pieces that teach the invention as claimed. "For example, Weban's reconfigurable network node "is a standalone board with an FPGA, a bootstrap loader PLD, SRAM, ROM, and network line drivers and receivers"" The FPGA is consistent with all interpretations of the "programmable" claimed limitation, and the I/O on the device is reconfigurable as shown in sections 7 and 8 of Weban. Furthermore the master slave relationship as found in section 8 where there are two FPGA's used together forming the reconfigurable network measuring tool is another valid interpretation of Applicant's claimed invention taught by Weban.

The remainder of Applicant's arguments are directed toward and hinge upon the definition of the claimed limitations addressed in the objection above, and the argument regarding claim 1. As such those arguments are traversed for the same reasons as set forth above.

Regarding claim 2, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry utilizing the hardware

architecture file [Wenban: A complete FPGA configuration file can be downloaded over the network in to the SRAM using these messages (Page 36, left column, second paragraph)].

Regarding claim 3. the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches creating a reconfigurable circuitry configuration file which describes a configuration for the reconfigurable circuitry;

wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry utilizing the reconfigurable circuitry configuration file [Wenban: A complete FPGA configuration file can be downloaded over the network in to the SRAM using these messages (Page 36, left column, second paragraph)].

Regarding claim 4, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches wherein the block diagram includes a first portion that specifies a configuration for the programmable hardware element, and wherein the block diagram includes a second portion that specifies a configuration for the reconfigurable circuitry; wherein said generating comprises generating the hardware architecture file based on the first portion of the block diagram; and wherein said configuring the reconfigurable circuitry comprises configuring the reconfigurable circuitry based on the second portion of the block diagram [Fountain: page 8, and page 9] These pages teach a modular, multilevel design of various portions, for various hardware items.

Claim 5, and 6 contains similar limitations as claim 4, thus is rejected for the same reasons as claim 4.

Regarding claim 7, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches wherein the reconfigurable circuitry comprises reconfigurable digital circuitry [Wenban: EDIF].

Regarding claim 8, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches wherein the reconfigurable circuitry comprises reconfigurable analog circuitry [Wenban: AHDL].

Claim 9 combines the limitations of claims 7 and 8, thus are rejected for the same reasons as claims 7 and 8.

Regarding claim 10, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches wherein the device also includes a processor and memory coupled to the programmable hardware element; the method further comprising: storing an executable program in the memory of the device for execution by the processor on the device, wherein the executable program operates with the programmable hardware element and the reconfigurable circuitry to perform the measurement function [Wenban: A complete FPGA configuration file can be

downloaded over the network in to the SRAM using these messages (Page 36, left column, second paragraph)].

Regarding claim 11, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches wherein the device also includes a processor and memory coupled to the programmable hardware element; wherein the hardware architecture file is based on a first portion of the block diagram; the method further comprising: generating an executable program based on a second portion of the block diagram; storing the executable program in the memory of the device for execution by the processor on the device [Wenban: Bootstrap page 36].

Regarding claim 12, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches wherein the device is coupled to a computer system; wherein said creating, said generating, and said configuring are performed in response to software executing on the computer system [Wenban: page 33,6 Interfaces, PC AT computer].

Regarding claim 13, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches wherein the block diagram comprises a graphical program [Fountain: Page 8].

Regarding claim 14, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches wherein the block diagram comprises a portion of a graphical program, wherein the graphical program also includes a display portion [Fountain: page 8].

Regarding claim 15, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches displaying one or more panels on a display during the programmable hardware element in the device executing to perform the measurement function on the signal, wherein at least one of the one or more panels displays the measured signal [Fountain: page 10].

Claims 16-21 contain further limitations found in National Instruments Lab View software taught by Fountain, as a virtual instrument.

Regarding claim 22, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches wherein the device operates as an instrument [Fountain: Downloaded virtual instrument as described by the combination]; wherein the external source is a unit under test [Wenban: Page 35-36, 8 Example].

Regarding claim 23, the combination as applied to claim 1, teaches the method of claim 1. The combination further teaches further comprising: at least one of the programmable hardware element and the reconfigurable circuitry generating a stimulus

signal to the unit under test prior to the device acquiring the signal from unit under test [Wenban: Page 35-36, 8 Example].

Claims 24 and 25 contain the similar limitations as claims 7 and 8 respectively thus are rejected for the same reasons as claims 7 and 8.

Claim 26 contains a combination of the limitations gathered from claims 1-23, thus the limitations present in claim 26 are rejected for the same reasons as those found in claims 1-23 with similar limitations.

Claims 27-30 contains a combination of the limitations gathered from claims 1-23, thus the limitations present in claim 26 are rejected for the same reasons as those found in claims 1-23 with similar limitations. The difference between the two sets of claims is the configuration information, that is further defined as a hardware architecture file as provided for in claim 2.

Claims 31-55 contain the system of method claims 1-23, thus are rejected for the same reasons as claims 1-23.

Claims 56-63 contain a combination of the limitations gathered from claims 1-23, thus the limitations present in claim 56-63 are rejected for the same reasons as those found in claims 1-23 with similar limitations.

Claims 64-85 differ from claims 1-23, by the automation function being described by the block diagram instead of the measurement function of claim 1. The combination as applied to claim 1 is not limited to the measurement function as the Wenban provides for any function to be programmed. Further the speciation does not provided the

difference between a measurement function and an automation function which would differentiate the claims, therefore claims 64-85, are rejected for the same reasons as claims 1-23.

Claims 86-108 are the system for method claims 64-85, thus are rejected for the same reasons as claims 64-85.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke Osborne whose telephone number is (571) 272-4027. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571) 272-3753. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LRO

Paul L. Rodriguez
Supervisory Patent Examiner
Art Unit ~~2125~~ 2123

4/3/06